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TOLER & LARSON & ABEL L.L.P.			ORTIZ, EDGARDO	
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Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)			
Office Action Summary		10/691,212	DORNBUSCH ET AL.			
		Examiner	Art Unit			
		Edgardo Ortiz	2815			
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1)⊠	Responsive to communication(s) filed on 21 O	<u>ctober 2003</u> .				
2a)	This action is FINAL . 2b)⊠ This	·				
3)	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposit	ion of Claims					
4) Claim(s) 1-29 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) is/are allowed. 6) Claim(s) 1-29 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or election requirement.						
Applicat	ion Papers					
9)☐ The specification is objected to by the Examiner.						
10)[10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.					
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).					
11)[Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.					
Priority (under 35 U.S.C. § 119					
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
2) Notice 3) Information	ce of References Cited (PTO-892) the of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) ter No(s)/Mail Date 10/21/03.	4) Interview Summary Paper No(s)/Mail D 5) Notice of Informal B 6) Other:				

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 2-7 and 9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 2 and its dependent claims 3-7 disclose the limitation "first predetermined amount corresponds to an attenuation in a stopband of said first external filter" and Claim 9 discloses "first and second predetermined amounts correspond to differences between an attenuation in stop-bands of said first and second filters respectively". However, Applicant has failed to provide sufficient support in order to enable someone with ordinary skill to correlate the predetermined distance between the first and second terminal pairs of independent Claim 1 to the attenuation in a stop-band of the first external filter disclosed in said Claim 2. Based on the evidence, the specification, at the time the application was filed, would not have taught one skilled in the art how to make and/or use the full scope of the claimed invention without undue experimentation.

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 2 discloses a "first predetermined amount" when describing the separation between the first and second terminal pairs, however, Claim 1 from which Claim depends from discloses a "first predetermined distance". Thus, the subject matter of Claim 2 is unclear in relation to the claim which it depends from, since it discloses an amount instead of a distance.

Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poulin (U.S. Patent No. 6,580,163) in view of Williams (U.S. Patent No. 3,868,608). With regard to Claim 1, Poulin discloses (figure 2) an integrated circuit (column 3, lines 6-7) comprising:

a semiconductor substrate (102) having a first pair of bonding pads from the plurality of bond pads defined as (106) and a second pair of bonding pads also from said plurality of bonding pads; and

an integrated circuit package (104) encapsulating said semiconductor substrate (102) and having first and second terminal pairs from the group defined as (108) corresponding and coupled to the first and second pairs of bonding pads, respectively,

wherein said first and second terminal pairs are separated by a first predetermined distance, which maintains isolation therebetween of at least a predetermined amount.

Poulin fails to teach the claimed input of the first external filter and output of the first external filter. However, Williams discloses (figure 2) a surface wave filter structure, which includes symmetrical input (28) and output terminals (30, 32) deposited over a substrate (34) and that is used in a frequency selective circuit (column 1, lines 54-56). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Poulin to include the claimed input of the first external filter and output of the first external filter, as suggested by Williams, in order to provide a surface wave filter with a high degree of symmetry and which exhibits improved attenuation at pre-selected frequencies (column 1, lines 57-61).

With regard to Claim 2, a further difference between the claimed invention and Poulin is the claimed first predetermined amount corresponding to attenuation in a stop-band of said first external filter. However, Williams discloses (figure 2) a surface wave filter structure, which includes symmetrical input (28) and output terminals (30, 32) deposited over a substrate (34) and wherein the input and output transducers are arranged symmetrically to sufficiently balance the parasitic effects between the output signals (column 3, lines 57-61). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Poulin to include the claimed first predetermined amount corresponding to an attenuation in a stop-band of said first external filter, as suggested by Williams, in order to

provide a surface wave filter with a high degree of symmetry and which exhibits improved attenuation at pre-selected frequencies (column 1, lines 57-61). Moreover, it is a known principle that the attenuation of the stop-band corresponds to the input frequency to the terminals and thus the separation of the terminals would be an obvious optimization to the ordinary artisan, in order to maintain a desired frequency constant.

With regard to Claim 3, Poulin discloses a first pair of terminals from the plurality of terminals defined as (108) and a second pair of terminals also from said plurality of bonding pads, located along a first side, which can be seen as any of the four sides of said integrated circuit package (104), and separated by a first plurality of intervening terminals (see figure 2).

With regard to Claim 4, a further difference between the claimed invention and Poulin is the claimed first plurality of intervening terminals comprising twelve terminals. However, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Poulin to include the claimed first plurality of intervening terminals comprising twelve terminals, in order to maintain a constant number of terminals through-out the semiconductor package and between the input and output terminals, thus reducing cross-signaling and improving isolation. Further, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to determine the intervening terminals as twelve, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

With regard to Claim 5, the limitation "wherein said first plurality of intervening terminals comprises at least one power supply", is an intended-use limitation that does not structurally or

patentably distinguish the claimed invention from the structure as disclosed by Poulin.

With regard to Claim 6, Poulin discloses first and second terminals of said first terminal pair are

adjacent to one another, and first and second terminals of said second terminal pair are adjacent

to one another (see figure 1).

With regard to Claim 7, Poulin discloses first and second terminal pairs are located at opposite

ends of said first side of said integrated circuit package (see figure 2).

With regard to Claim 8, Poulin discloses an integrated circuit wherein:

the semiconductor substrate (102) further has a third pair of bonding pads, from the

plurality of bonding pads (106) and a fourth pair of bonding pads, also from the plurality of

bonding pads;

an integrated circuit package (104) having third and fourth terminal pairs, from the group

of terminals (108) corresponding and coupled to said third and fourth pairs of bonding pads,

respectively; and

said third and fourth terminal pairs are separated by a second predetermined distance.

Poulin fails to teach the claimed input of the first external filter and output of the first external filter. However, Williams discloses (figure 2) a surface wave filter structure, which includes symmetrical input (28) and output terminals (30, 32) deposited over a substrate (34) and that is used in a frequency selective circuit (column 1, lines 54-56). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Poulin to include the claimed input of the first external filter and output of the first external filter, as suggested by Williams, in order to provide a surface wave filter with a high degree of symmetry and which exhibits improved attenuation at pre-selected frequencies (column 1, lines 57-61).

With regard to Claim 9, a further difference between the claimed invention and Poulin is the claimed first predetermined amount corresponding to attenuation in a stop-band of said first external filter. However, Williams discloses (figure 2) a surface wave filter structure, which includes symmetrical input (28) and output terminals (30, 32) deposited over a substrate (34) and wherein the input and output transducers are arranged symmetrically to sufficiently balance the parasitic effects between the output signals (column 3, lines 57-61). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Poulin to include the claimed first predetermined amount corresponding to an attenuation in a stop-band of said first external filter, as suggested by Williams, in order to provide a surface wave filter with a high degree of symmetry and which exhibits improved attenuation at pre-selected frequencies (column 1, lines 57-61). Moreover, it is a known principle that the attenuation of the stop-band corresponds to the input frequency to the terminals and thus

the separation of the terminals would be an obvious optimization to the ordinary artisan, in order to maintain a desired frequency constant.

With regard to Claim 10, Poulin discloses a first pair of terminals from the plurality of terminals defined as (108) and a second pair of terminals also from said plurality of bonding pads, located along a first side, which can be seen as any of the four sides of said integrated circuit package (104), and separated by a first plurality of intervening terminals (see figure 2).

With regard to Claim 11, a further difference between the claimed invention and Poulin is the claimed first plurality of intervening terminals comprising twelve terminals. However, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Poulin to include the claimed first plurality of intervening terminals comprising twelve terminals, in order to maintain a constant number of terminals through-out the semiconductor package and between the input and output terminals, thus reducing cross-signaling and improving isolation. Further, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to determine the intervening terminals as twelve, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

With regard to Claim 12, the limitation "wherein said first and second pluralities of intervening terminals each comprises at least one power supply", is an intended-use limitation that does not

structurally or patentably distinguish the claimed invention from the structure as disclosed by Poulin.

With regard to Claim 13, Poulin discloses first and second terminals of each first, second, third, and fourth terminal pairs that are adjacent to one another (see figure 2).

With regard to Claim 14, Poulin discloses first and second terminal pairs located at opposite ends of said first side of said integrated circuit package and said third and fourth terminal pairs are located at opposite ends of said second side of said integrated circuit package, wherein the terminals comprise terminals from the group defined as (108) (see figure 2).

With regard to Claim 15, Poulin discloses (figure 2) an integrated circuit (column 3, lines 6-7) comprising:

a semiconductor substrate (102) having first, second, third and fourth quadrants, which can be seen as those portions between an horizontal and a vertical line taken along the substrate, having respective first, second, third and fourth bonding pads defined as (106) and a second pair of bonding pads also from said plurality of bonding pads and first and second circuit portions on the semiconductor substrate; and

an integrated circuit package (104) encapsulating said semiconductor substrate (202) and having first, second, third and fourth terminal from the group defined as (108) corresponding and coupled to the first, second, third and fourth bonding pads, respectively.

Poulin fails to teach the claimed input of the first external filter and output of the first external filter. However, Williams discloses (figure 2) a surface wave filter structure, which includes symmetrical input (28) and output terminals (30, 32) deposited over a substrate (34) and that is used in a frequency-selective circuit (column 1, lines 54-56). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Poulin to include the claimed input of the first external filter and output of the first external filter, as suggested by Williams, in order to provide a surface wave filter with a high degree of symmetry and which exhibits improved attenuation at pre-selected frequencies (column 1, lines 57-61).

With regard to Claim 16, Poulin discloses first and second circuits that comprise portions of radio-frequency (RF) receivers (column 3, lines 6-8).

With regard to Claim 17, the limitation "wherein said first circuit comprises a portion of a satellite receiver and said second circuit comprises a portion of a terrestrial receiver", is an intended-use limitation that does not structurally or patentably distinguish the claimed invention from the structure as disclosed by Poulin.

With regard to Claim 18, Poulin discloses first and second circuits that have substantially the same layout (see figure 2).

With regard to Claim 19, Poulin fails to disclose the claimed first and second external surface acoustic wave (SAW) filters. However, Poulin fails to teach the claimed input of the first external filter and output of the first external filter. However, Williams discloses (figure 2) a surface wave filter structure, which includes symmetrical input (28) and output terminals (30, 32) deposited over a substrate (34) and that is used in a frequency selective circuit (column 1, lines 54-56). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Poulin to include the claimed first and second external surface acoustic wave (SAW) filters, as suggested by Williams, in order to provide a surface wave filter with a high degree of symmetry and which exhibits improved attenuation at pre-selected frequencies (column 1, lines 57-61).

With regard to Claim 21, Poulin discloses (figure 2) an integrated circuit (column 3, lines 6-7) comprising:

a semiconductor substrate (102) having a first pair of bonding pads from the plurality of bond pads defined as (106) and a second pair of bonding pads also from said plurality of bonding pads; and

an integrated circuit package (104) encapsulating said semiconductor substrate (102) and having at least first and second sides, and comprising a first pair of terminals from the group defined as (108) located at a first end of said first side and coupled to said first pair of bonding pads, and a second pair of terminals located at a second end of said first side opposite said first end and coupled to said second pair of bonding pads (see figure 2).

With regard to Claim 22, Poulin discloses an integrated circuit package (104) that comprises four sides (see figure 2).

Page 12

With regard to Claims 23, 24 and 27; Poulin and Williams essentially disclose the claimed invention but fails to explicitly show, the claimed thin quad-flat package. However, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Poulin and Williams to include the claimed thin quad-flat package, in order to optimize the overall size of the device, since TQFP are space-efficient resulting in smaller printed circuit board space requirements.

With regard to Claim 25, Poulin discloses semiconductor substrate further having a third pair of bonding pads, from the group defined as (106), and a fourth pair of bonding pads, also from the group defined as (106), and said integrated circuit package further has a third pair of terminals from the group defined as (108) located on a first end of said second side and coupled to said third pair of bonding pads, and a fourth pair of terminals located on a second end of said second side opposite said first end and coupled to said fourth pair of bonding pads.

Poulin fails to teach the claimed input of the first external filter and output of the first external filter. However, Williams discloses (figure 2) a surface wave filter structure, which includes symmetrical input (28) and output terminals (30, 32) deposited over a substrate (34) and that is used in a frequency selective circuit (column 1, lines 54-56). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the

structure as disclosed by Poulin to include the claimed input of the first external filter and output of the first external filter, as suggested by Williams, in order to provide a surface wave filter with a high degree of symmetry and which exhibits improved attenuation at pre-selected frequencies (column 1, lines 57-61).

With regard to Claim 26, Poulin discloses (figure 2) an integrated circuit (column 3, lines 6-7) comprising:

adjacent first and second terminals from the group defined as (108) at a first end of a first side of the integrated circuit;

adjacent third and fourth terminals, also from the group defined as (108), at a second end of said first side of the integrated circuit;

adjacent fifth and sixth terminals, also from the group defined as (108), at a first end of a second side of the integrated circuit; and

adjacent seventh and eighth terminals, also from the group defined as (108), at a second end of said second side of the integrated circuit.

With regard to Claim 28, a further difference between the claimed invention and Poulin is, the claimed assignment of pin numbers to the terminals. However, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to assign pin numbers to the terminals for the purpose of defining and identifying which operation each terminal would perform within the integrated circuit.

With regard to Claim 29, Poulin fails to disclose the claimed first and second external surface acoustic wave (SAW) filters. However, Poulin fails to teach the claimed input of the first external filter and output of the first external filter. However, Williams discloses (figure 2) a surface wave filter structure, which includes symmetrical input (28) and output terminals (30, 32) deposited over a substrate (34) and that is used in a frequency selective circuit (column 1, lines 54-56). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Poulin to include the claimed first and second external surface acoustic wave (SAW) filters, as suggested by Williams, in order to provide a surface wave filter with a high degree of symmetry and which exhibits improved attenuation at pre-selected frequencies (column 1, lines 57-61).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Application/Control Number: 10/691,212 Page 15

Art Unit: 2815

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3/17/05

TOM THOMAS SUPERVISORY PATENT EXAMINER